What is claimed is:

1. A collar dielectric process, comprising the steps of:

providing a semiconductor silicon substrate having a deep trench and a deep trench capacitor, in which the deep trench capacitor comprises a node dielectric formed on the sidewall and bottom of the deep trench and a storage node formed in the deep trench and reaching a predetermined depth;

performing an ion implantation process to form an ion implantation area on the substrate at the top of the deep trench;

removing the node dielectric until the top of the node dielectric is leveled off with the top of the storage node, thus exposing the sidewall of the deep trench outside the deep trench capacitor; and

performing an oxidation process to grow a first silicon oxide layer on the exposed sidewall of the deep trench, in which the first silicon layer is outside the ion implantation area.

2. The collar dielectric process as claimed in claim 1, wherein the ion implantation process uses N_2 as the ion source to restrain the growth of the first silicon oxide layer.

3. The collar dielectric process as claimed in claim 1, wherein the position and vertical length of the ion

implantation area corresponds to those of a buried strap outdiffusion region.

4. The collar dielectric process as claimed in claim 1, wherein the ion implantation process partially surrounds a partial top of the deep trench and is adjacent to a buried strap outdiffusion region.

5. The collar dielectric process as claimed in claim 1, wherein the ion implantation process entirely surrounds the top of the deep trench.

6. The collar dielectric process as claimed in claim 1, wherein the vertical length of the ion implantation area is 800~1500Å.

7. The collar dielectric process as claimed in claim 1, wherein the node dielectric is a silicon nitride layer.

8. The collar dielectric process as claimed in claim 1, wherein the storage node is an n^+-doped polysilicon layer.

9. The collar dielectric process as claimed in claim 1, wherein the deep trench capacitor further comprises a buried plate which is an n^+-type diffusion region formed in the substrate at the lower portion of the deep trench and surrounding the node dielectric.

10. The collar dielectric process as claimed in claim 1, further comprising the steps of:

forming a second silicon oxide layer on the sidewall of the deep trench to cover the first silicon oxide layer and the ion implantation area;

forming a first conductive layer in the deep trench to connect the top of the storage node;

recessing the first conductive layer until reaching a predetermined depth; and

etching the second silicon oxide layer and the first silicon oxide layer to level off the top of the second silicon oxide layer and the top of the first silicon oxide layer until the top of the first conductive layer protrudes from the tops of the second silicon oxide layer and the first silicon oxide layer, wherein the combination of the second silicon oxide layer and the first silicon oxide layer remaining on the sidewall of the deep trench serve as a collar dielectric layer.

11. The collar dielectric process as claimed in claim 10, wherein the first conductive layer is an n^+-doped polysilicon layer.

12. The collar dielectric process as claimed in claim 10, further comprising the steps of:

forming a second conductive layer in the deep trench; and

forming a buried strap outdiffusion region in the silicon substrate adjacent to the second conductive layer, wherein the position and vertical length of the buried strap outdiffusion

region correspond to those of the ion implantation area.

13. The collar dielectric process as claimed in claim 12, wherein the second conductive layer is a polysilicon layer.

14. The collar dielectric process as claimed in claim 12, wherein the buried strap outdiffusion region is an n^+-type diffusion region.